SPECIFICATION

Please replace the summary of the invention on page 2, line 12 through page 3, line 29, with the following replacement summary of the invention.

We describe ~~A feature of the present invention is to provide~~ a semiconductor integrated circuit capable of selectively providing output signals to test semiconductor integrated circuits by means of a test device having less pins than the semiconductor integrated circuits it tests.

And we describe ~~Another feature of the present invention is to provide~~ a test method of a semiconductor integrated circuit by means of a test device having less pins than the semiconductor integrated circuits it tests.

A ~~According to an aspect of the present invention, a~~ semiconductor integrated circuit includes a plurality of data output pins, a data processing circuit to generate output signals responsive to an input signal, and an output selection circuit with at least a normal mode and a test mode. A first group of output signals are provided to a first group of data output pins in a first test cycle of the test mode. And a second group of output signals are provided to a second group of data output pins during a second test cycle of the test mode.

In an embodiment, the test cycles of the output selection circuit are repeated during the test mode.

In an embodiment, the output selection circuit repeats the first and second test cycles during testing.

In an embodiment, the output selection circuit sends ith output signals (i being a positive integer) to ith data output pins during the first cycle of the test mode. And the output selection circuit sends (i+1)th output signals to ith output pins during the second test cycle of the test mode.

In an embodiment, the output selection circuit sends ith output signals (i being a positive integer) to (i+1)th data output pins during the first cycle of the test mode. And the output selection circuit sends the (i+1)th output signals to (i+1)th output pins during the second test cycle of the test mode.

~~In an embodiment, the output selection circuit sends first to (N/2)th output signals (N being an integer) to first to (N/2)th data output pins during the first cycle of the test mode. And~~

~~the output selection circuit sends ((N/2)+1)th to Nth output signals to first to (N/2)th output pins during a second test cycle of the test mode.~~

~~In an embodiment, the output selection circuit sends the first to (N/2)th output signals (N being a integer) to the ((N/2)+1)th to Nth data output pins during the first cycle of the test mode. And the output selection circuit sends the ((N/2)+1)th to Nth output signals to the ((N/2)+1)th to Nth output pins during the second test cycle of the test mode.~~

A ~~According to another embodiment, a~~ method for outputting data during a test mode of a semiconductor integrated circuit having a plurality of data output pins is provided. The method includes sending some output signals to a first group of the data output pins and sending remaining output signals to the first group of the data output pins.

In an embodiment, the sending some output signals and the sending remaining output signals are repeated during a test mode.

In an embodiment, the sending some output signals includes sending ith output signals (i being a positive integer) are sent to ith data output pins.

In an embodiment, i is a positive odd integer.

In an embodiment, the sending remaining output signals includes sending (i+1)th output signals (i being a positive integer) to ith data output pins.

~~In an embodiment, the sending some output signals includes sending first to (N/2)th output signals (N being a positive integer) to first to N/2th data output pins.~~

~~In an embodiment, the sending remaining output signals includes sending ((N/2)+1)th to Nth output signals are sent to the first to (N/2)th data output pins.~~

~~In an embodiment, the sending some output signals includes sending first to (N/2)th output signals (N being a positive integer) to the ((N/2)+1)th to Nth data output pins.~~

~~In an embodiment, the sending remaining output signals includes sending ((N/2)+1)th to Nth output signals to the ((N/2)+1)th to Nth data output pins.~~